GLAST ACD Readout Controller (GARC) Review
July 2, 2002

- Description of GARC
- Block diagram of core logic
- Description of Verilog, Exemplar, and L-Edit Toolsets
- GARC Functionality vs. Level IV Requirements, ICD
- Verilog Code
- GARC schematics
- Test plan for GARC

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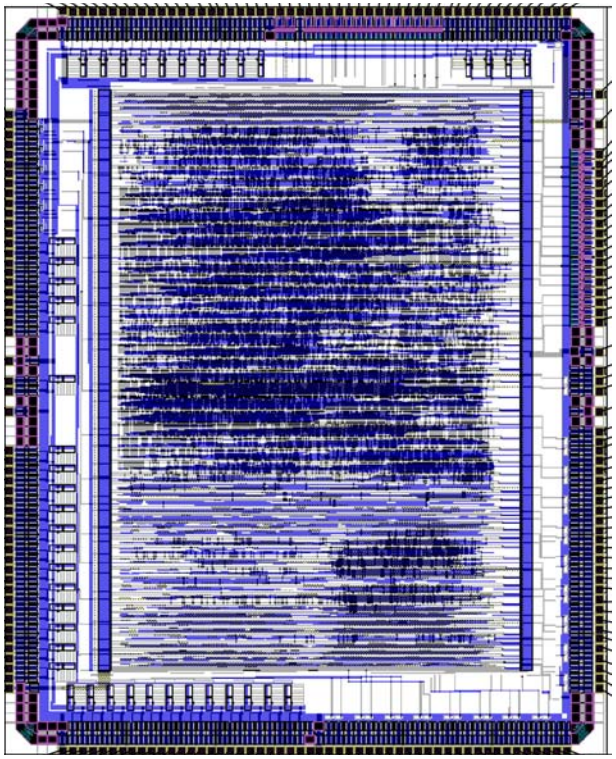
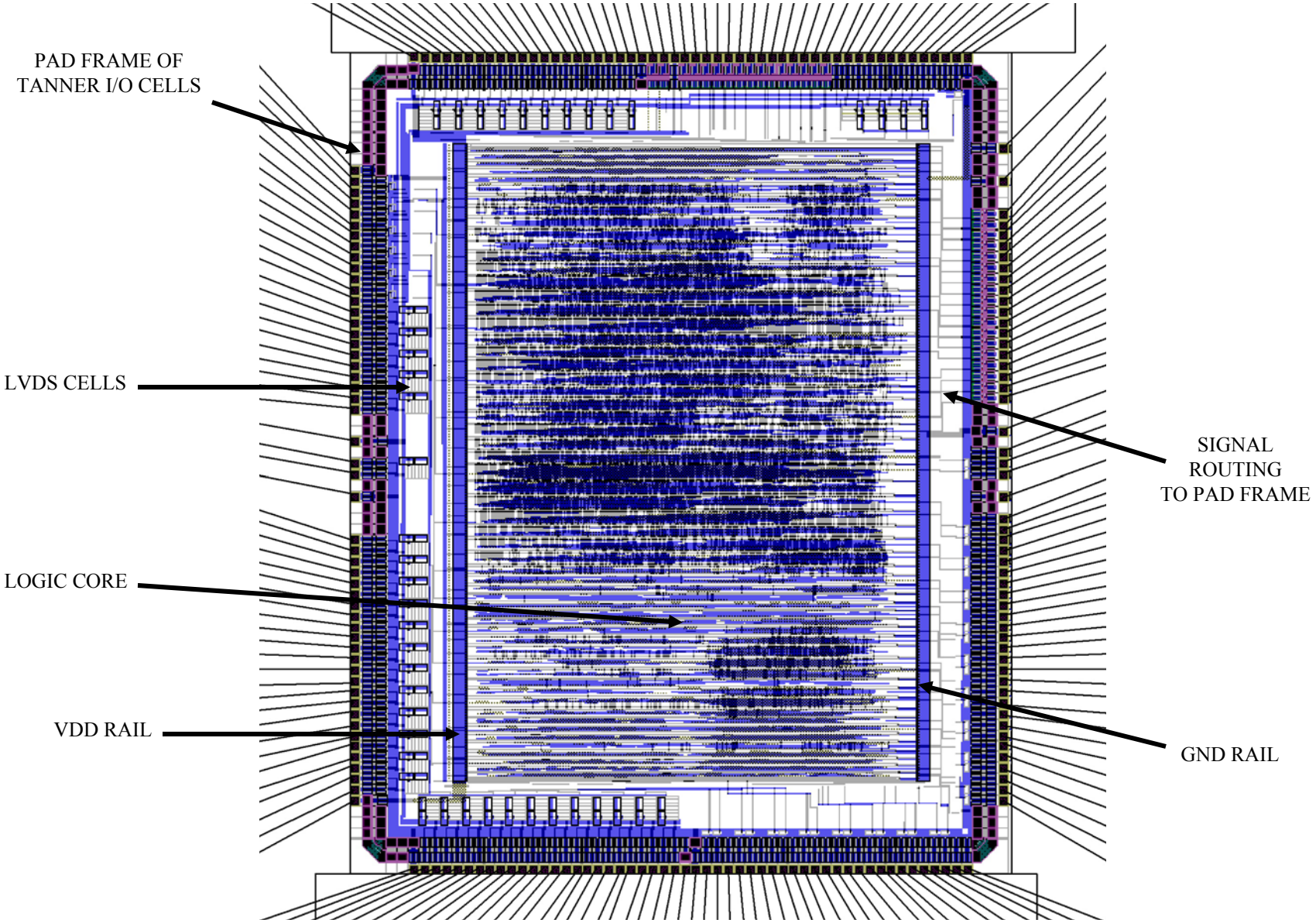
ACD GARC Version 1

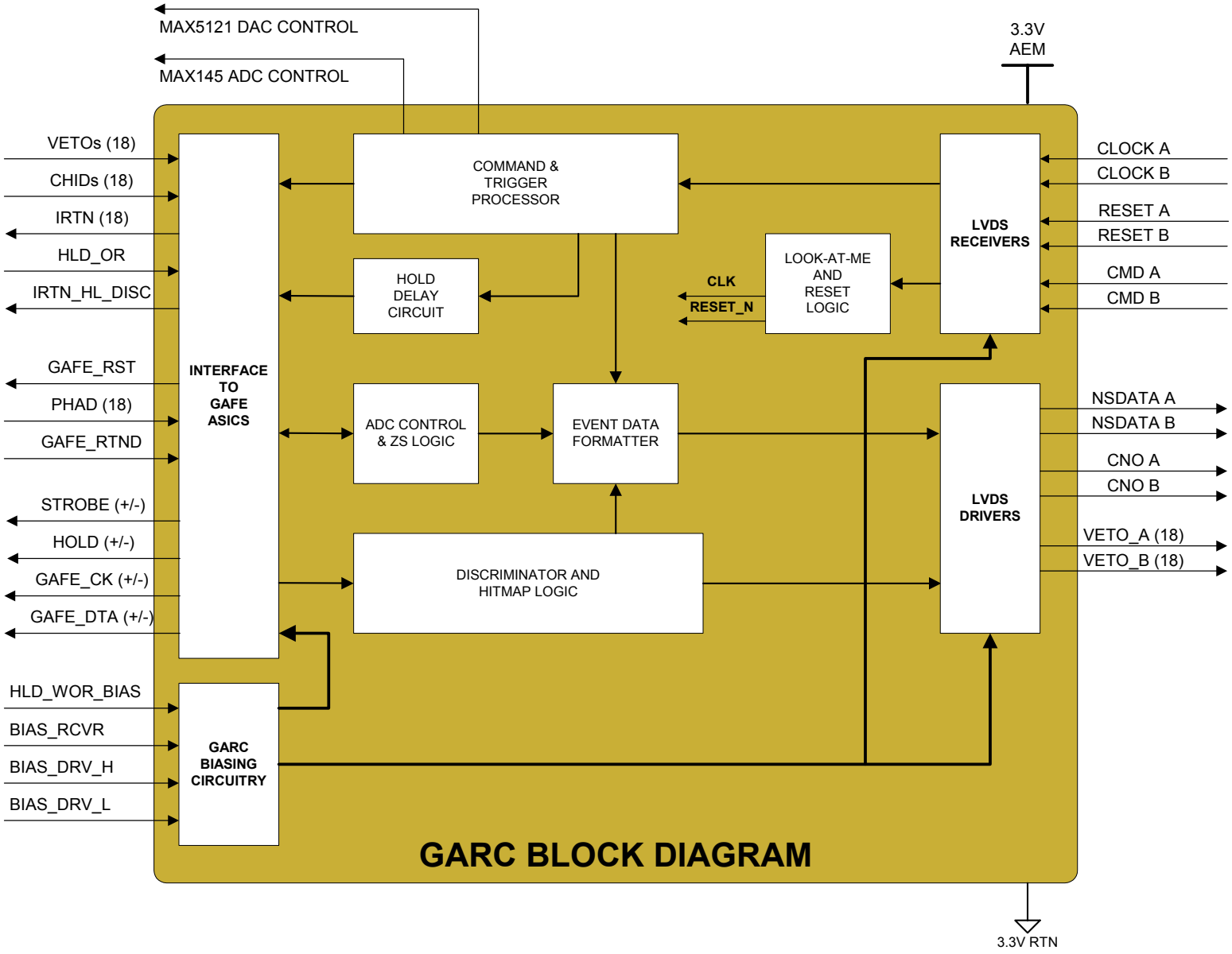


- Main Functions
  - Command processor to receive configuration from the AEM
  - Telemetry formatter to distribute data to the AEM
  - PHA state machine to control the FREE circuit card's ADCs and provide the zero-suppression function
  - Current-Mode LVDS interfaces to the AEM for digital signals
  - Current-Mode lower power pseudo-differential interfaces to the GAFE ASICs
  - HitMap register for the VETO and CNO discriminators
- Near-term plans
  - 1st generation ASIC is in fabrication now
  - Start testing ASIC when received in August
  - 2nd generation ASIC sent to foundry in late September
- Flight Quantity: 12 GARC ASICs to be flown

GARC Physical Layout



GARC Block Diagram



Discussion of GARC Design

(based on information in the Electrical Specification)

1. Clock and Reset circuitry
2. Die pinouts and I/O cell description
3. Plastic packaging
4. LVDS I/O modules
5. Analog ASIC (GAFE) interface modules
6. Biasing resistors
7. Look-at-Me logic (Primary vs. Secondary AEM selection)
8. VETO and HitMap processing
9. Command processor and formats
10. Event Data formatter and formats
11. ACD and zero-suppression logic
12. ADC interface
13. DAC interface
14. Trigger operation
15. HVBS operation
16. Cal Strobe operation

Tools Utilized for GARC Design & Verification

1. **Verilog** (coding HDL, initial simulation via testbench)

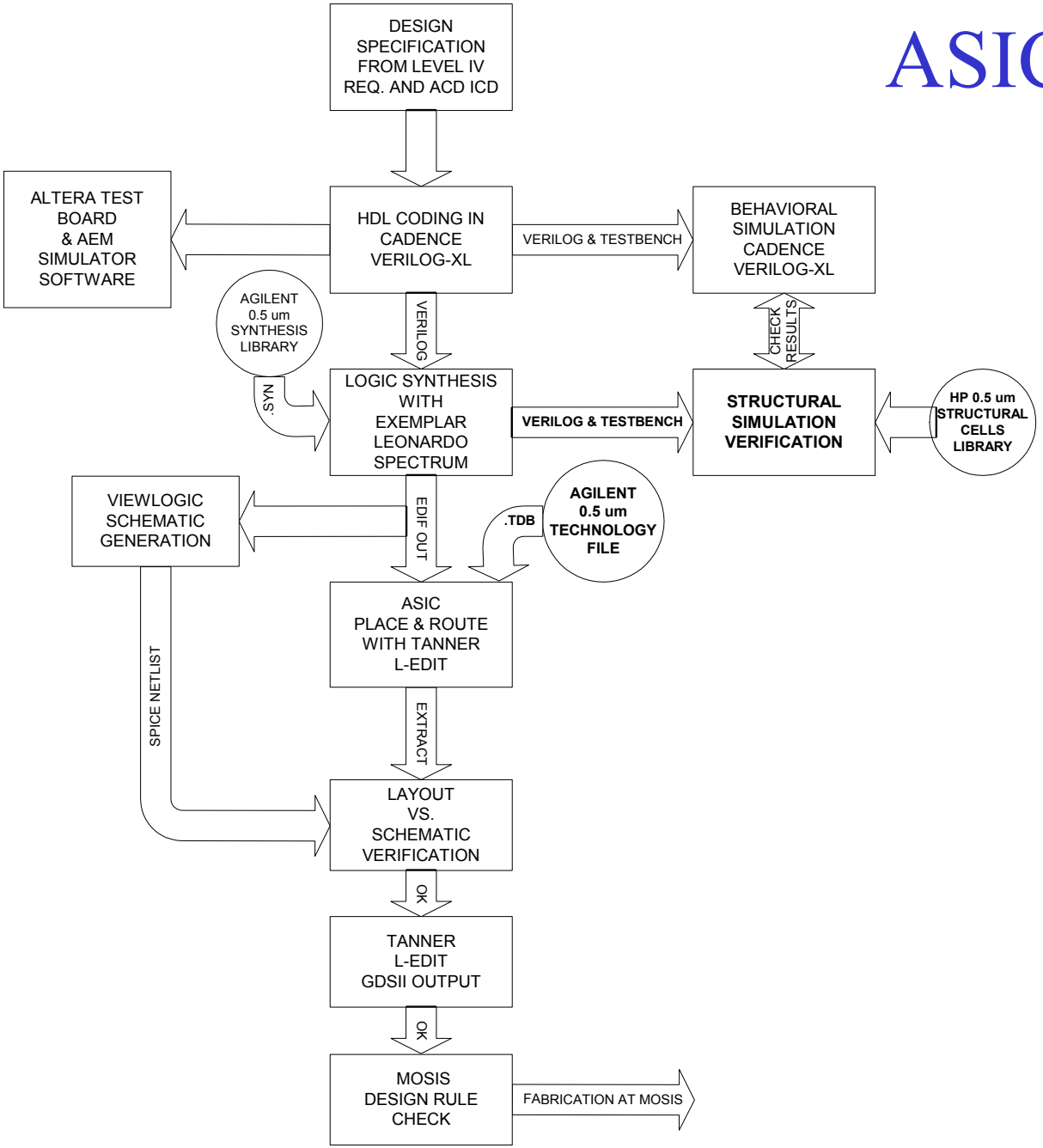
2. Exemplar **Leonardo Spectrum** (logic synthesis) and synthesis to Altera FPGA for real-time emulation

3. Tanner **L-Edit** (physical layout)

4. Tanner **LVS** and **DRC** (layout vs. schematic, DRC)

5. MOSIS Design Rule Check (final check vs. foundry rules)

ASIC Design Flow



GARC Test Plan Overview

- Check all register commands (configuration write & configuration read)
- Check functionality of all dataless commands (i.e., HV, Reset, Calib, etc.)
- Check functionality and timing of each VETO signal (ext. pulse generator)
- Check functionality and timing of the HitMap
- Check operation of ZS and Non-ZS Trigger commands
- Check operation of MAX145 ADCs
- Check operation of MAX5121 DAC
- Verify LVDS drivers and receivers
- Test operation of Look-At-Me logic
- Verify operational ranges of GARC biasing circuitry
- Verify voltage/power ranges
- Verify operation over LAT/ACD temperature ranges (GARC test board)

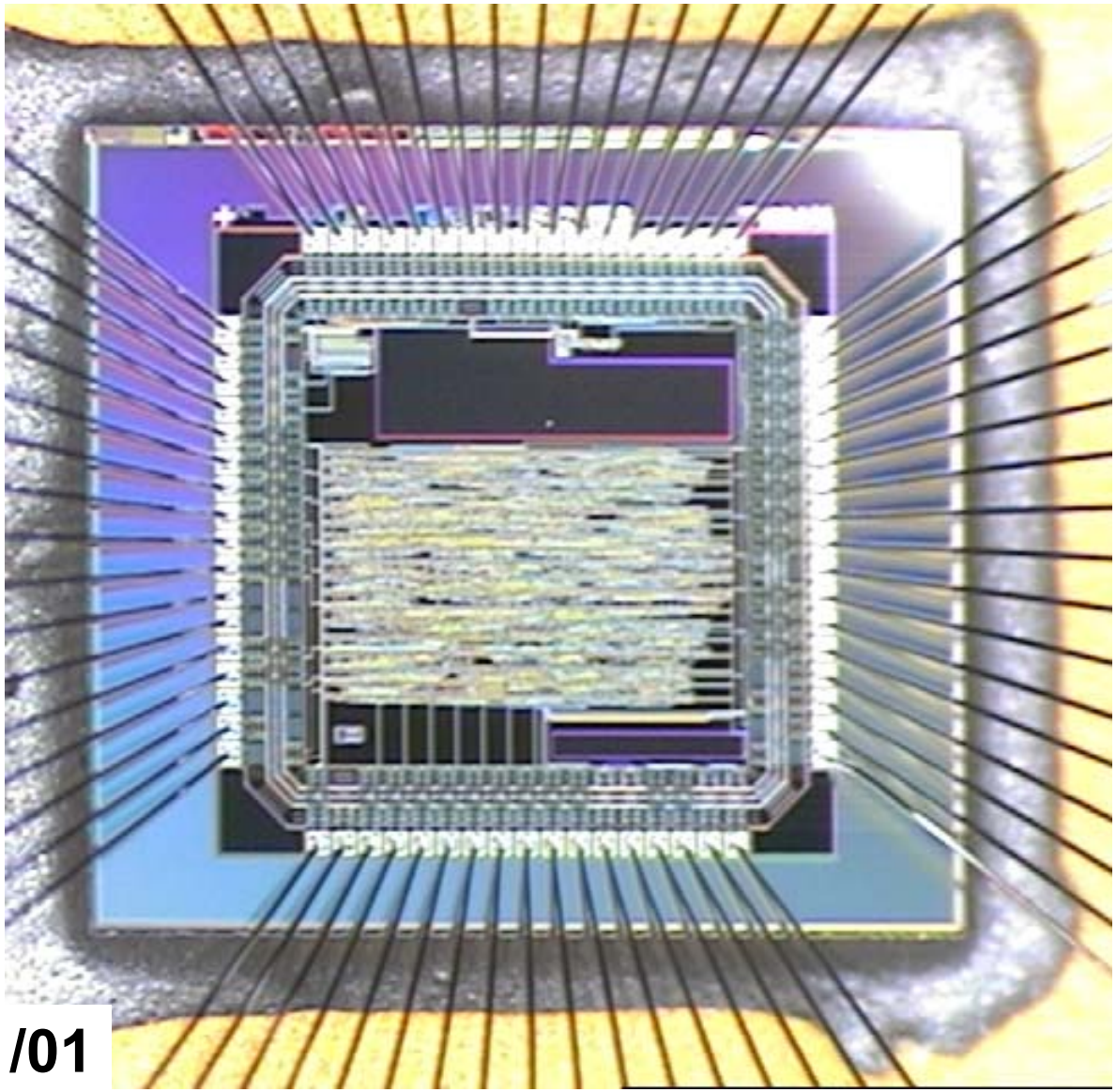
- Test results to be compared to specifications in AEM-ACD ICD

Possible Items for Discussion

1. MTEST Test ASIC done with Tanner
2. Design vs. ICD, Level IV Requirements
3. Verilog code – clock, reset, overall logic design techniques
4. GARC Schematics
5. GARC Logic Core Block Diagram
6. Testing Plan

MTEST Test ASIC

- **Purpose of "MTEST"**
  - **Verify Exemplar synthesis and Tanner layout toolsets, process to transfer GDSII data from LHEA to MOSIS, MTEST logic module, ESD protection pads and Tanner I/O buffers**
  - **Test 101-stage ring oscillator, DAC, LVDS drivers and poly-resistors**



Tested at GSFC 11/01